Terms used **instruction trace data miss** OR **cache miss** Found **350** of **171,143**

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1 Comprehensive multiprocessor cache miss rate generation using multivariate models
Ilya Gluhovsky, Brian O'Krafka
May 2005 **ACM Transactions on Computer Systems (TOCS)**, Volume 23 Issue 2
Publisher: ACM Press
Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, references, index terms

This article presents a technique for taking a sparse set of cache simulation data and fitting a multivariate model to fill in the missing points over a broad region of cache configurations. We extend previous work by its applicability to multiple miss rate components and its ability to model a wide range of cache parameters, including size, associativity and sharing. Miss rate models are useful for broad design exploration in which many cache configurations cannot be simulated directly due to l ...

Keywords: Additive models, cache miss rates, extrapolation, isotonic regression, queuing models

2 Expected I-cache miss rates via the gap model
R. W. Quong
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2
Publisher: IEEE Computer Society Press, ACM Press
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index terms

To evaluate the performance of a memory system, computer architects must determine the miss rate m of a cache C when running program P. Typically, the measured miss rate depends on the specific address mapping M of P set arbitrarily by the compiler and linker. In this paper, we remove the effect of the address-mapping on the miss rate by analyzing a symbolic trace T of basic blocks. By assuming each basic block has an equal probability of ending up anywhere in the address map, we determine the e ...

3 Memory optimization for embedded systems: Improved indexing for cache miss reduction in embedded systems
Tony Givargis
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(215.59 KB) Additional Information: full citation, abstract, references, index terms

The increasing use of microprocessor cores in embedded systems as well as mobile and portable devices creates an opportunity for customizing the cache subsystem for

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PowerPC 603 Microprocessor -- Page 2

... is loaded from the instruction cache (or external memory on a **cache miss**). ... In the trace mode of operation, **instruction tracing** or branch tracing is ...
www-03.ibm.com/servers/eserver/ pseries/hardware/whitepapers/power/ppc_603_2.html - 27k - Cached - Similar pages

[PDF] Performance Analysis and Tracing of Technical and Java ...

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tool that allows the **instruction tracing** of applications. It. works on the kernel level, ... **cache miss** rates of large technical applications are almost ...
min.ecn.purdue.edu/~hassanin/ papers/ispass_2003_paper.pdf - Similar pages

Hardware mechanism for instruction/data address tracing - Patent ...

An improved **instruction tracing** mechanism provides a combination of hardware ... In machines that depend on low **cache miss** rates, the cache inhibited scheme ...
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[DOC] Modeling:

File Format: Microsoft Word - View as HTML
Much of our modeling methodology depends on **instruction tracing** to acquire application ... Initial results, using **cache miss** rates as the prediction target, ...
perc.nersc.gov/reports/PERC-2-model-report.doc - Similar pages

[PPT] Add title here

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event-based counters: MIPS, IA64, Pentium; ProfileMe **instruction tracing**: Alpha ... multiple metrics for each program line; computed metrics, eg **cache miss** ...
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[PDF] October 15, 2002 12:46 WSPC/123-JCSC 00061 CODE COVERAGE-BASED ...

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similar effect on load latencies (ie per-static-load **cache miss** rates) ... TRIP6000 **instruction tracing** tool. TRIP6000 is an early version of ...
www.ece.umd.edu/courses/enee759m.S2000/ papers/lipasti1996-asplos7.pdf - Similar pages

[PPT] Slide 1

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m5/mem/**cache/miss/***. Blocking buffer. Used to simulate a blocking cache; Speeds simulation in atomic ... DPRINTF and Tracing; **Instruction Tracing**. rundiff ...
m5.eecs.umich.edu/dist/tutorial.ppt - Similar pages

[PS] additional features such as non-blocking fetches [Kro81 ...

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A similar effect on load latencies (ie per-static-load **cache miss** ... traces are collected and

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Citations: Efficient **program tracing** - Larus (ResearchIndex)
Efficient **program tracing**. IEEE Computer, 26(5):52–61, May 1993. ... in which case the profile counts the number of times each path suffered a **cache miss**. ...
citeseer.ist.psu.edu/context/17213/0 - 32k - Cached - Similar pages

Trace-driven Memory Simulation: A Survey - Uhlig, Mudge ...
... 1994 11: **Cache miss** equations: An analytical representation of cache misses ... 1988 ACM DBLP 64 Efficient **program tracing** (context) - Larus - 1993 ACM DBLP 64 ...
citeseer.ist.psu.edu/3745.html - 46k - Supplemental Result - Cached - Similar pages
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[PS] June 8, 1993 1 Wisconsi nA rchitecturalResearc hTo olSet Mark D ...
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QPT is described in: [3] James R. Larus, "Efficient **Program Tracing**," IEEE ... lines and data structures with the appropriate **cache miss** statistics. ...
ftp.cs.wisc.edu/markhill/SPEC92/can93_warts.ps - Similar pages

[PDF] Wisconsin Architectural Research Tool Set
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3] James R. Larus, "Efficient **Program Tracing**," IEEE Computer, 26, 5, May 1993, ... lines and data structures with the appropriate **cache miss** statistics. ...
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1 plus hit index size; for each **cache miss** address, the record ... JR Larus, "Efficient **program tracing**," Computer, Vol. 26. No 5, pp. 52-61, May 1993. ...
cadal.cse.nsysu.edu.tw/publications/ paper/conference/tracer.pdf - Similar pages

[PDF] Function-Level Power Estimation Methodology for Microprocessors
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many times each function is executed, **cache miss** rate and pipeline. stalls. ... Efficient **Program Tracing**. IEEE Computer, Vol. 26, No. ...
www.ece.umd.edu/~gangqu/research/papers/c015.pdf - Similar pages

[PS] Operating System Impact on Trace-Driven Simulation Jason Casmira ...
File Format: Adobe PostScript - View as HTML
Table 3: **Cache miss** rates, with and without operating system overhead ... [19] J. Larus, "Efficient **Program Tracing**," IEEE. Computer Magazine, May 1993, pp. ...
www.ece.neu.edu/info/architecture/ publications/simulation.ps.gz - Similar pages

[PDF] Function-Level Power Estimation Methodology for Microprocessors
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... The **cache miss** rate usually depends on the cache specifications (cache size, associativities, replace ... v 0 1 v 0 2 v 0 m g ; Phase II: **program tracing** run the ...
sigda.org/Archives/ProceedingArchives/ Dac/Dac2000/papers/2000/dac00/pdffiles/49_4.pdf - Supplemental Result - Similar pages

[PS] Appears in: "Proceedings of the 1995 ACM SIGMETRICS Conference ...
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However, one program with a relatively large instruction **cache miss** ratio incurs ... Efficient **Program Tracing**. IEEE Computer, 26(5):52-61, May 1993. ...

Terms used **placeholder sequential** Found **19,211** of **910,869**

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1 The semantics of future and an application

C. Flanagan, M. Felleisen

January 1999 **Journal of Functional Programming**, Volume 9 Issue 1

Publisher: Cambridge University Press

Additional Information: full citation, abstract

The **future** annotation of MultiLisp provides a simple method for taming the implicit parallelism of functional programs. Prior research on **future** has concentrated on implementation and design issues, and has largely ignored the development of a semantic characterization of **future**. This paper considers an idealized functional language with **futures** and presents a series of operational semantics with increasing degrees of intensionality. The first semantics defines **fut ...**

2 Parallel execution of sequential scheme with ParaTran

Pete Tinker, Morry Katz

January 1988 **Proceedings of the 1988 ACM conference on LISP and functional programming**

Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a system called ParaTran for executing sequential Scheme in parallel. It supports arbitrary side effects without requiring user annotations. The ParaTran runtime system detects and corrects data dependency violations using an automatic history and rollback mechanism. ParaTran is first described by analogy with Time Warp, a system for distributed simulation; this description is followed by a discussion of ParaTran's implementation and presentation of pre ...

3 Safe futures for Java

Adam Welc, Suresh Jagannathan, Antony Hosking

October 2005 **ACM SIGPLAN Notices , Proceedings of the 20th annual ACM SIGPLAN conference on Object oriented programming systems languages and applications OOPSLA '05**, Volume 40 Issue 10

Publisher: ACM Press

Full text available: pdf(364.09 KB) Additional Information: full citation, abstract, references, index terms

A future is a simple and elegant abstraction that allows concurrency to be expressed often through a relatively small rewrite of a sequential program. In the absence of side-effects, futures serve as benign annotations that mark potentially concurrent regions of code. Unfortunately, when computation relies heavily on mutation as is the case in Java, its meaning is less clear, and much of its intended simplicity lost.This paper explores the definition and implementation of *safe* futures for ...